Freeform Search

Database: US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Term:

Display: 10 **Documents in Display Format:** - **Starting with Number** 1

Generate: ○ **Hit List** ◉ **Hit Count** ○ **Side by Side** ○ **Image**

Search Clear Interrupt

Search History

DATE: Thursday, December 22, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L33	l14 and l27	18	L33
	DB=USPT; PLUR=YES; OP=OR		
L32	(5539906 | 5153936 | 4933880 | 4495582 | 5978804 | 5440401 | 4688181 | 5553281 | 5584022 | 5875268 | 5276901 | 5666215 | 4799156 | 5852435 | 5263157 | 5065447 | 5315693 | 5319543 | 5493677 | 6154755 | 5784461 | 6017157 | 5426594 | 5630125 | 5463555 | 5696901 | 4992940 | 5319401 | 5319402 | 5144556 | 4956769 | 5625776 | 5845263 | 5469353 | 5581749 | 5383027)![PN]	36	L32
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L31	('6321231')[ABPN1,NRPN,PN,TBAN,WKU]	2	L31
L30	L29 and (copie$ or replicas)	10	L30
L29	L28 and host	15	L29
L28	L27 and (high and low) near2 resolution	49	L28
L27	L26 and (network or www or internet or web)	262	L27
L26	L25 and stor$ near facility	318	L26

L25	digital near image	75649	L25
L24	355/70	653	L24
L23	355/40	2586	L23
L22	355.clas.	35500	L22
L21	345/604	345	L21
L20	345/603	258	L20
L19	345/589	1338	L19
L18	345/428	1281	L18
L17	345/418	1944	L17
L16	345/302	1018	L16
L15	345/132	883	L15
L14	345.clas.	71174	L14
L13	705/42	623	L13
L12	705/33	115	L12
L11	705/27	2593	L11
L10	705/26	5583	L10
L9	705.clas.	38653	L9
L8	715/530	653	L8
L7	715.clas.	23629	L7
L6	707.clas.	31191	L6
L5	707/530	1290	L5
L4	707/104.1	5148	L4
L3	707/102	6723	L3
L2	707/10	11015	L2
L1	707/3	7743	L1

END OF SEARCH HISTORY

L33: Entry 14 of 18 File: USPT Jan 7, 1997

US-PAT-NO: 5592237
DOCUMENT-IDENTIFIER: US 5592237 A

TITLE: High resolution image processor with multiple bus architecture

DATE-ISSUED: January 7, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Greenway; William C.	Tully	NY		
Breithaupt; David	Dewitt	NY		
Schoppe; Donald W.	Bridgeport	NY		
Lutz; Norman M.	Liverpool	NY		
Beardslee; Andrew W.	Baldwinsville	NY		
Nguyen; Minh N.	Liverpool	NY		
Stevener; Timothy L.	Cicero	NY		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
InfiMed, Inc.	Liverpool	NY			02

APPL-NO: 08/334577 [PALM]
DATE FILED: November 4, 1994

INT-CL-ISSUED: [06] H04 N 5/907, H04 N 7/00

US-CL-ISSUED: 348/716; 348/718, 348/231, 348/552, 348/426, 345/200, 395/309
US-CL-CURRENT: 348/716; 345/531, 345/555, 348/231.9, 348/552, 348/718, 375/240.01, 710/317

FIELD-OF-CLASSIFICATION-SEARCH: 348/715, 348/716, 348/718, 348/719, 348/162, 348/231, 348/426, 348/555, 348/572, 348/552, 348/913, 345/189, 345/190, 345/200, 345/201, 395/309, 395/311, 395/312, 395/497.02, 395/164, 395/166, 358/909.1, H04N 5907, 700, H04N005/907., 7
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4868651	September 1989	Chou et al.	358/111

☐	5179582	January 1993	Keller et al.	378/96
☐	5220312	June 1993	Lumelsky et al.	345/200
☐	5452022	September 1995	Yamamoto et al.	348/231
☐	5481279	January 1996	Honda et al.	345/201
☐	5483296	January 1996	Nonweiler	348/715

ART-UNIT: 262

PRIMARY-EXAMINER: Peng; John K.

ASSISTANT-EXAMINER: Murrell; Jeffrey S.

ATTY-AGENT-FIRM: Trapani & Molldrem

ABSTRACT:

A multiple video data bus architecture permits high speed data transfer among the various circuit elements of a fluoroscopic imaging processor. This permits simultaneous acquisition, storage, display, and image enhancement of high resolution, i.e., 2K.times.2K images. A memory interface circuit compresses the video data for storage in bulk memory. The processor supports several high-resolution monitors which can respectively display radiographic images from different subjects, so that review and diagnosis can occur remotely.

9 Claims, 8 Drawing figures

Previous Doc Next Doc Go to Doc#

L33: Entry 14 of 18 File: USPT Jan 7, 1997

DOCUMENT-IDENTIFIER: US 5592237 A
TITLE: High resolution image processor with multiple bus architecture

Brief Summary Text (16):
An A/D converter circuit is responsible for converting the video image signals to a digital image signal as a sequence of digital bytes at a density of 2K bytes per line of the video image.

Brief Summary Text (17):
A memory interface circuit accepts flames of the digital image signal and conditions the same for writing it onto a bulk storage medium, e.g., magnetic disk memory. The memory interface circuit also reads out frames of the digital image signal from the bulk memory, and these two operations can occur simultaneously. The memory interface circuit includes data compression circuitry, such as standard JPEG compression buffering, for greater storage capacity and rapid reading from and writing to bulk memory.

Brief Summary Text (18):
An image processor circuit includes video memory means for storing first and second frames of the digital image signal, e.g. to use as a mask image and a subtractive image, for image enhancement. This processor also includes circuitry for image enhancement such as is described in U.S. Pat. No. 4,868,651-mentioned earlier, and non-linear image enhancement transform circuitry which can enhance the contrast and show up faint details in the video image. A crossbar switch provides data connection between a data bus interface and the various image enhancement and memory means on this circuit board.

Brief Summary Text (19):
A display interface circuit is responsible for providing the video image signal to an associated image display device (i.e. a monitor or a hard copy printer), including on-board memory for temporarily storing at least one frame of the input digital image signal, and buffering means that provides the video image signal to the display device at a frame rate that is not dependent on the frame rate of the digital image signal being supplied to the display interface circuit. In practice, the arrangement includes several display interface circuits, so various images can be displayed at the same time on different monitors or displays.

Brief Summary Text (21):
These circuits can be implemented on boards which plug into a back plane that contains a digital control bus and multiple parallel data buses, each of which is independently addressable. The multiple data bus architecture permits the high speed simultaneous transfer of various different frames of the digital image signal between the other components boards. In a preferred embodiment there are five (5) parallel independently addressable data buses, and each of the A-D circuit board (s), the display interface circuit board, the image pipeline processor board, and the memory interface board has a five fold data bus interface circuit connecting to respective nodes of each of the five data buses. These boards also couple to the control bus as do the system controller circuit board and the user interface board. Additional data buses can be implemented in the back plane.

Detailed Description Text (2):
With reference to FIG. 1 of the Drawing, a video imaging digital fluoroscope arrangement 10 is shown with a human patient 12 lying horizontally on a stage or table 14. An X-ray tube 16 beneath the table receives high voltage impulses from an X-ray generator 18, and emits radiation which passes through a collimator 20 and then through the body tissues of the patient 12, to fall on an image intensifier 22. The latter produces a fluorescent image that passes through focusing and aperture optics 24 and is picked up by a video camera 26. In this case, the camera contains a high-resolution camera tube 28. This camera produces a video signal which is then fed to a fluoroscopic image processor, i.e. a digital video processor 30. The processor is coupled to a system controller 32 which provides control signals for aperture control of the optics 24 and also for level and timing of the high voltage from the generator 18. A number of external devices are connected to the processor 30, and these include a control room key pad 34 and control room monitor 36, the monitor 36 having a high-resolution screen. A storage device, e.g., a magnetic disk unit 38, serves as a bulk storage facility for the high-resolution digital images processed in the processor 30. The processor is also coupled to a hard copy machine 40, which produces radiographic images on paper or if preferred on film. A remote key pad 42 and a remote monitor 44 also coupled to the digital video processor 30 can be located in a second room to permit viewing of images e.g. images reproduced from those stored on the magnetic storage facility 38. In order to obtain the highest possible resolution, the camera tube 28 achieves resolution, in this case, of approximately 2048.times.2048 pixels.

Detailed Description Text (6):
In order to handle the large volume of digital data associated with each image, i.e., 4 megabytes per image, at an acceptable rate of data transfer, the digital video processor 30 has a multiple data bus architecture. In this architecture there are five imaging buses employed to interconnect circuit board resources. The data flow connectivity shown in FIGS. 2 and 3 provides a flexible interconnect network which makes it possible to perform multiple image processing operations simultaneously. For example, with the processor 30 it is possible to display real time images as they are being acquired, while at the same time an image processor performs image subtraction or image data manipulations from other stored images, and displays them on a separate monitor.

Detailed Description Text (9):
A block diagram of the A-D interface board 58 is shown in FIG. 4. Here, a capacitor 90 provides AC coupling of the analog video input, through a buffer 92. Field, vertical, and horizontal synchronizing signals are stripped in a sync stripper module 94. The horizontal synchronizing signals are fed to a voltage controlled oscillator 96 and also to a crystal oscillator 98, both of which have outputs applied to a clock-select multiplexer 100. A clock signal and the video input signal are each fed to a 10 bit A-D converter 102, whose output is supplied as a digital image signal which is fed through a multiplexer 103 to a video memory that is comprised of a first video dynamic RAM 104 and a second video dynamic RAM 106 connected in parallel. Each of the VDRAMs 104 and 106 stores one complete 2K.times.2K frame of the video signal, and as a digitized video signal. The video output signal is applied, from each VDRAM 104, 106 alternately to a backplane transceiver logic interface 108, which sends the digitized video signal to a selected one of the BTL buses, 72, 74, 76, 78, 80.

Detailed Description Text (18):
A first compression channel 165 has inputs coupled respectively to the multiplexer/demultiplexer 164 and comprises an odd line channel 166, a even line channel 168, and a bit strip channel 170. In a preferred embodiment, digital image data is provided as 10-bit bytes. The eight most significant bits of the even line bytes are supplied to the even line channel, and the eight most significant bits from the odd-line bytes are supplied to the odd-line channel 168. The two least significant bits, from two odd line bytes and two even-line bytes, are combined

into eight-bit bytes. These go to the bit strip channel 170.

Detailed Description Text (22):
The control bus 200 and the image and overlay memories 206, 108 are connected to inputs of a video output device or RAMDAC 212. This output device 212 converts the digital images into a high resolution (2048 line) output video signal, which can be supplied to a high resolution video signal, which can be supplied to a high resolution monitor at refresh rates high enough to eliminate flicker.

Current US Class (1):
345

CLAIMS:

1. High resolution digital image storage and processing arrangement for capturing, storing, enhancing and displaying a series of video images produced by a high resolution video imager that delivers image signals having a density of 2048 lines per frame and for furnishing said video image signals to a high resolution image display device, comprising:

a) A/D circuit means for converting said video image signals to a digital image signal as a sequence of digital bytes at a density of 2048 pixels per line of said video image signal;

b) display circuit means for providing said video image signal to said image display device including onboard memory means for temporarily storing at least one frame of said digital image signal, and buffering means for providing said video image signal to said display device at a frame rate independent of the frame rate of the digital image signal supplied to said display circuit means;

c) image processor circuit means including video memory means for storing at least one frame of said digital image signal and image enhancement means for creating an enhanced video image based on the digital image signal stored in said video memory means;

d) memory interface circuit means for writing frames of said digital image signal onto a bulk data storage medium and for reading frames of the digital image signal from said storage medium;

e) system controller means for generating control signals to control flow of said digital image signal between the A/D circuit means, said display circuit means, said image processor circuit means and said memory interface circuit means;

f) a user interface device permitting a user to select an operational mode, and means generating a control signal based on the operational mode selected;

g) a digital control bus coupled to said A/D circuit means, said display circuit means, said image processor circuit means, said memory interface circuit means, said system controller means and said user interface device for carrying control signals between said system controller means and said A/D circuit means, said display circuit means, said image processor circuit means, and said memory interface circuit means; and

h) a plurality of parallel independently addressable data buses each of which is coupled to a respective data bus interface on each of said A/D circuit means, said display circuit means, said image processor circuit means, and said memory interface circuit means.

2. High resolution digital image storage and processing arrangement according to claim 1, wherein said plurality of data buses includes five BTL data buses, and

each of said A/D circuit means, said display circuit means, said image processor circuit means, and said memory interface circuit means includes five BTL bus interface circuits connected to respective data ports of said BTL data buses.

3. High resolution digital image storage and processing arrangement according to claim 1 wherein said display circuit means includes an on-board video image memory, means coupling said on-board video image memory to an associated bus interface device for receiving the digital image signal from any of said plurality of data buses; a video processor coupled to said on-board video image memory and to a control bus interface that is coupled to said digital control bus; and a video output device having data input means coupled to said video image memory and control input means coupled to said video processor, and an output supplying a high-resolution output video signal to an associated display device to produce a high resolution image thereon.

4. High resolution digital image storage and processing arrangement according to claim 3, said display circuit means further including image synchronizer means for generating a vertical frame rate for said output video signal that is independent of the rate at which the digital image signal is supplied over said bus interface device to said video image memory.

5. High resolution digital image storage and processing arrangement according to claim 3, wherein said display circuit means further includes an overlay image memory coupled to said video output device and a text and graphics generator coupled to said overlay image memory for generating overlay text and graphics so that said video output device generates said output video signal with text and graphics superimposed on said high resolution image.

6. High resolution digital image storage and processing arrangement according to claim 1, wherein said image processor circuit means includes non-linear image enhancement transform means for transforming the stored digital image signals to produce an enhanced video image.

7. High resolution digital image storage and processing arrangement according to claim 6, wherein said image processor circuit means includes a control bus interface coupled to said digital control bus; data bus interface means coupled to said plurality of data buses; and crossbar switch means coupled to said control bus interface, said data bus interface means, said non-linear image enhancement transform means, and said means for storing at least two frames of said digital image signal.

8. High resolution digital image storage and processing arrangement according to claim 1, wherein said memory interface circuit means includes data compression means for converting said digital image signal to a compressed form for recording the recorded signal to a decompressed form when played back from said bulk data storage medium.

9. High resolution digital image storage and processing arrangement according to claim 8, wherein said data compression means includes first and second channels for compressing and recording a frame of said video image signal, and simultaneously playing back and decompressing another frame of said video image signal.

Previous Doc Next Doc Go to Doc#